


ACKNOWLEDGEMENT RECEIPT

Electronic Version

Stylesheet Version v01

Title of Invention	STRUCTURE AND METHOD OF MAKING STRAINED SEMICONDUCTOR CMOS TRANSISTORS HAVING LATTICE-MISMATCHED SOURCE AND DRAIN REGIONS																																																																																																						
Submission Type :	Utility Patent Filing																																																																																																						
Application Number:	10/604607																																																																																																						
EFS ID:	44758																																																																																																						
Server Response:	<table border="1"> <thead> <tr> <th>Confirmation Code</th> <th>Message</th> </tr> </thead> <tbody> <tr> <td>ISVR1</td> <td>Submission was successfully submitted - Even if Informational or Warning Messages appear below, please do not resubmit this application</td> </tr> <tr> <td>ICON1</td> <td>1606</td> </tr> <tr> <td>IGEN77</td> <td>Filename= FIS920030199US1-usfees.xml BusinessRule= The access code is not included which allows for automated processing to the deposit account.</td> </tr> </tbody> </table>			Confirmation Code	Message	ISVR1	Submission was successfully submitted - Even if Informational or Warning Messages appear below, please do not resubmit this application	ICON1	1606	IGEN77	Filename= FIS920030199US1-usfees.xml BusinessRule= The access code is not included which allows for automated processing to the deposit account.																																																																																												
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First Named Applicant:	Huajie Chen																																																																																																						
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